WE CLAIM:

1. A method for forming a MOS transistor gate dielectric layer comprising:

providing a semiconductor substrate;

forming an oxide layer on the semiconductor substrate;

exposing the oxide layer to a high-density nitrogen plasma to incorporate nitrogen into the oxide layer thereby converting the oxide layer to an oxynitride layer; and

annealing said oxynitride layer in N_2O to form an oxynitride layer with a uniform nitrogen concentration profile.

2. The method of claim 1 wherein the exposing the oxide layer to a high-density nitrogen plasma comprises a plasma power level of 700 - 900 watts.

3. The method of claim 1 wherein annealing the oxynitride layer in N_2O comprises rapid thermal annealing at a temperature of 800°C - 1100°C for 10-60 seconds.

4. A method of forming a MOS transistor comprising:

providing a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate wherein the gate dielectric layer has a uniform nitrogen concentration;

forming a conductive layer on said gate dielectric layer,

forming sidewall structures adjacent to said conductive layer; and

forming source and drain regions in the semiconductor substrate adjacent to said sidewall structures.

5. The method of claim 4 wherein said forming a gate dielectric layer with a uniform nitrogen concentration comprises:

forming an oxide layer on the semiconductor substrate;

exposing the oxide layer to a high-density nitrogen plasma to incorporate nitrogen into the oxide layer thereby converting the oxide layer to an oxynitride layer; and

annealing said oxynitride layer in N_2O to form an oxynitride layer with a uniform nitrogen concentration profile.

6. The method of claim 5 wherein the exposing the oxide layer to a high-density nitrogen plasma comprises a plasma power level of 700 - 900 watts.

7. The method of claim 5 wherein annealing the oxynitride layer in N_2O comprises rapid thermal annealing at a temperature of 800°C - 1100°C for 10-60 seconds.

8. The method of claim 4 wherein said uniform nitrogen concentration is greater than 6 atomic percent.

9. The method of claim 4 wherein gate dielectric layer is less than 40 angstroms thick.

10. The method of claim 4 wherein said uniform nitrogen concentration describes a nitrogen concentration with less than 10% variation across the gate dielectric layer.

11. A MOS transistor, comprising:

providing a silicon substrate;

a gate dielectric layer on the silicon substrate wherein the gate dielectric layer is less than 40 angstroms thick and wherein the gate dielectric layer has a uniform nitrogen concentration;

a conductive layer on the gate dielectric layer;

sidewall structures adjacent to said conductive layer; and

source and drain regions in the silicon substrate adjacent to the sidewall structures.

12. The MOS transistor of claim 10 wherein the uniform nitrogen concentration is greater than 6 atomic percent.

13. The MOS transistor of claim 12 wherein the uniform nitrogen concentration has a variation of less than 10% across the gate dielectric layer.